Remarks

Claims 1-68 were pending in this Application. Claims 1-34 were Elected with Traverse in the response filed on **04/28/2006**. The Restriction Requirement having been made Final, Applicant hereby Cancels Claims 35-68. Claims 20, 27 and 28 have been Rejected under 35 U.S.C. 112 as failing to comply with the written description requirement, and Claims 1-34 have been Rejected based on 35 U.S.C. 103(a) as being unpatentable over Rajavel, *et al.*, U.S. Patent 5,742,089 [hereinafter Rajavel] in view of Han, *et al.* U.S. Patent 7,056,471 [hereinafter Han] and Mitra, U.S. Patent 6,208,005 [hereinafter Mitra]. In addition, the Examiner has requested Applicant to provide a copy of the Chen *et al.* article cited on its IDS; stating that the copy thereof has not been received and was not considered.

It appears that the Examiner may not have reviewed the·Application as Amended by the Preliminary Amendment Filed on **27 May 2004**, which Amended Claims 27-32, 34, 37, 39, 46-49, 52, 53, 55 and 57. This Amendment is reflected in the File Wrapper available on Private PAIR and Applicant's Attorney notes that the Examiner has not indicated that that Preliminary Amendment has been Rejected and not entered.. In fact, the Examiner indicated in the Restriction Requirement that the Restriction Requirement was in Response to the Communication Filed on **27 May 2004**, *i.e.*, the Preliminary Amendment not the Patent application which was Filed on **19 March 2004**. Applicant respectfully requests the Examiner to withdraw the Rejection of Claims 27 and 28 and to the extent that Claims 27 and 28 and Claims 29-34 which Depend from Claim 28, apparently, were not examined on their merits as Amended, Applicant Respectfully requests that the next Examination be treated as a First Examination on the merits in the event of any further Objections or Rejections that might otherwise result in a Final Rejection.

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Copy of Article Cited in IDS

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Applicant apologizes for the Examiner not having received a copy of the cited IDS article. Applicant's Attorney hand carried copies of the two cited U.S. Patents as well as the Chen Article listed on the IDS as document AC to the Attorney Window on Thursday 27 May 2004 at approximately 11:50 PM, and the Date Stamped Transmittal Sheet shows that I Filed a 34 page Paper. This Paper included the Transmittal Sheet (1 page), the Preliminary Amendment (13 pages), an IDS Cover Sheet (2 pages), PTO Forms 08A (1 page) and 08B (1 page), U.S. Patent 5,306,386 de Lyon (5 pages), U.S. Patent 5,399,206 de Lyon (6 pages) and the Chen Article (5 pages) for a total of 34 pages. NOTE: As that article was available on-line on 22 March 2003 and dispatched in the printed journal on 4 April 2003, this article is NOT a 35 U.S.C. 102 statutory bar in regard to the instant Application. However, as the article states, "[The Applicants] have reported for the first time the successful MBE growth of CdScTe on Si lattice matched to LWIR HgCdTe."

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Claim Rejection 35 U.S.C. 112

Specifically

The Examiner states that

> Claims 20, 27, 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

> "and z is greater ..." in claim 28 is erroneous since the film in question is $CdSe_xTe_{1-x}$. The antecedent basis for "the cadmium chalcogenide" in claim 20 appears to correspond to claim 19, not claim 14. (not quite clear here?) in claim 27 is unclear or erroneous.

Response

As indicated above, Applicant had Amended Claim 27 in the Preliminary Amendment to delete the language "(not quite clear here?)" and Amended Claim 28 to indicate a film in question of "CdS_xTe_{1-x}" rather than "$CdSe_xTe_{1-x}$." Claim 20 has been herein Amended to Depend from Claim 13 rather than Claim 14. Claim 28 has been further Amended herein to delete the language "~~inclusive and z is greater than zero and less than one.~~" and to end with inclusive.

Claim Rejection 35 U.S.C. 103(a)

The Examiner states that

> Claims 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajavel in view of Han and Mitra.

Specifically

The Examiner states that

> Re claims 1, 2, 21, Rajavel 5,742,089 teaches multilayer structure comprising a silicon based substrate 14, epitaxial layer 18 including II-VI semiconductor material including combination of two binary alloys such as CdSe/ZnTe but lacks the specific recitation regarding the composition, e.g., of $Cd_{1-z}Zn_zSe_xTe_{1-x}$. The provision of overlayer 20, e.g., HgCdTe is also taught. See column 3 line 45 to column 8 line 65.

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Response

Applicant notes that the reference to "column 3, line 45 to column 8, line 65" is apparently in error since Column 8 ends at line 52. Moreover, Applicant notes that this reference is to essentially the entire Specification of the referenced citation from "SUMMARY OF THE INVENTION" to the end of the Claims. Interestingly Column 1, line 65 to Column 2, line 6 is later cited. Applicant repeats Column 1, line 65 to Column 2, line 16 for the Examiner's convenience:

> A third approach has been to deposit untwinned CdZnTe layer on a ZnTe film grown on Si substrates (e.g. deLyon et al. Appl. Phys. Lett., vol. 63, 818(1993)). However, the crystalline quality of CdZnTe is not as good as that of CdTe layers deposited on Si because of phase separation problems. In addition, **CdTe is not lattice-matched to HgCdTe, which results in the generation of dislocations in the detector structure which degrade its performance.** Despite its lattice mismatch with silicon of about 18 percent, a $Cd_{0.96}Zn_{0.04}Te$ epilayer deposited on Si substrates is fully relaxed at the growth temperature, because of the generation of misfit dislocations. **However, when the CdZnTe/ZnTe/Si structure cools from the growth temperature to room temperature, the difference in the thermal expansion coefficients produces unequal contractions in the epilayer and the substrate, which creates a biaxial tensile stress in the epilayer.** This biaxial tensile stress induces the creation of additional dislocations. Furthermore, relatively high growth temperature of CdZnTe which is in excess of 250.degree. C. is an intrinsic limitation. **(emphasis added)**

And Column 7, lines 29-37

> Because the $Hg_{1-x}Cd_xTe$ materials are fully miscible with CdTe for all composition, **the structural perfection of $Hg_{1-x}Cd_xTe$ films is consistently better than that of CdZnTe and often exceeds that of CdTe films. In contrast, the crystalline quality of epitaxially grown $Cd_{1-x}Zn_xTe$ (x.apprxeq.0.04) is inferior to that of CdTe because the material is prone to phase separation as the composition deviates from that of the end point binaries. (emphasis added)**

In essence, Rajavel recognizes some of the specific problems with the existing art that Applicant's invention focuses on overcoming. See Paragraph [0004]:

> [0004] However, to advance this technology to long wavelength (LWIR, 8-12 μm) HgCdTe devices, lattice matching to HgCdTe is needed in order to reduce the dislocation density within the material. This is specifically necessary for LWIR material since an elevated dislocation density has a greater impact on device performance in the LWIR limit than in either MWIR or SWIR regions due to the inherently smaller band gap of long wavelength detecting HgCdTe material. To

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mitigate the lattice mismatch issue, initial efforts have focused on incorporating 4.3% Zn into the CdTe/Si layer to provide $Cd_{0.957}Zn_{0.043}Te/Si$ composite substrates which arc exactly lattice matched to LWIR HgCdTe. However, it is difficult to grow CdZnTe layers of suitable crystal quality and low defect levels on Si. Furthermore, the crystalline structure of $Cd_{1-z}Zn_zTe$ degrades for increasing values of z, perhaps due to a miscibility gap.

The method of growth of the epitaxial $Cd_{1-z}Zn_zX_xX'_{1-x}$ film grown on the silicon based substrate, as claimed in Claim 1 is what makes the multilayer patentable since following the teaching of Rajavel, a person of ordinary skill in the art would not be motivated to epitaxially grow such a film on the silicon based substrate because of phase separation and a lack of lattice matching which would result in the generation of dislocations and "degrade the performance." Applicant, however, in the method of manufacture disclosed in the Application and the subject of non-Elected method Claims 35-68 has provided both the motivation for fabricating a multilayer structure that the existing prior art would teach away from and Claimed specifically the multilayered structure to include both the silicon based substrate and the specific epitaxially grown film.

The Examiner's reference to Han:

> Han 7056,471 B1 teaches homogeneous II-VI quarternary [sic] alloys M1-xM2xAyB1-y having improved characteristics and easy to produce. .including the specific recitation of $Zn_{1-x}Cd_xSe_yTe_{1-y}$. The selection of the indices to be between zero and 1 is also taught. See the abstract, column 1 line 5 et seq., column 3 line 60 et seq., column 4 line 4 to column 9 line 65.

provides neither the motivation to combine the two references that the Examiner concludes would be "obvious to one skilled in the art in practicing the above invention to have selected the quaternary compounds as claimed since such quaternary compounds are conventional, advantageous and easy to produce as evidenced by Han."

Han was interested only in making nanocrystals with a high luminescence and stability. See Column 3, line 60 through Column 4, line 17.

> Therefore, there is still the necessity for nanocrystals with high luminescence and stability in aqueous solution, that are also easy to produce. There also remains the need for blue-emitting quantum dots which are useful as short-wavelength light-emitting devices. Consequently, it also remains a major goal to develop new synthetic methods or strategies of producing highly luminescent stable QDs, especially blue-emitting ones.

> Accordingly, it is an object of the invention to overcome the limitations of the prior art and to provide **nanocrystals that meet the above needs.**

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This object is solved by the nanocrystals and the processes of producing nanocrystals having the features of the respective independent claims.

In one embodiment such a nanocrystal is a nanocrystal consisting of a homogeneous ternary alloy having **the composition M1.sub.1-xM2.sub.xA, wherein a) M1 and M2 are independently selected from an element of the subgroup IIb, subgroup VIIa, subgroup VIIIa, subgroup Ib or main group II of the periodic system of the elements (PSE), when A represents an element of the main group VI of the PSE, or b) M1 and M2 are independently selected from an element of the main group (III) of the PSE, when A represents an element of the main group (V) of the PSE. (emphasis added)**

Han thus discloses a huge number of possible nanocrystals providing no guidance to anyone of ordinary skill in the art to make a specific quaternary compound as applicant has Claimed in Claim 1. Moreover, Han discloses a method of manufacturing nanocrystals of the micro alloys and does not disclose a method of making an epitaxial film of the quaternary compound nor is there any indication that producing nanocrystals would in any way overcome the problems of lattice mismatch or the degradation of the crystalline structure of the layers of suitable crystal quality and low defects on a silicone substrate.

Han makes only one reference to such "quaternary nanoalloys" in Column 7, line 22-26:

In the quaternary nanoalloys of the invention the same elements are present. Examples of quaternary alloys are Zn.sub.1-xCd.sub.xSe.sub.yTe.sub.1-y, Zn.sub.1-xCd.sub.xSe.sub.yS.sub.1-y, Hg.sub.1-xCd.sub.xSe.sub.yS.sub.1-y, Hg.sub.1-xCd.sub.xSc.sub.yTe.sub.1-y. (II-VI-nanoalloys) or Ga.sub.1-xIn.sub.xP.sub.yAs.sub.1-y (III-V-nanocrystals).

Again, there is no indication how to form such quaternary nanoalloys on a silicon substrate nor is there the motivation to do so, since, again, Han's motivation for producing the compounds was for "high luminescence and stability in aqueous solution" not for any ability to be used as an epitaxial layer on a silicon substrate.

The Examiner states that

Additionally, such variation would have been further obvious and advantageous as evidenced by Mitra, 6,208,005, column 5 line 60-65 wherein the variation of the alloy composition would have been conventional and obvious to obtain the desired film characteristics, e.g., desired bandgap.

Note that Mitra is drawn to mercury-based quaternary alloys. Applicant's Invention is providing a non-mercury epitaxially grown film on a silicon substrate. While Mitra does disclose various mercury based compounds that can affect the bandwidth of the

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semiconductor; as Applicant stated in Paragraphs [0003] and [0004], it is not for the short or medium bandwidths that this Applicant's invention is needed but for long wavelengths: "However, to advance this technology to long wavelength (LWIR, 8-12 μm) HgCdTe devices, lattice matching to HgCdTe is needed in order to reduce the dislocation density within the material." There is nothing disclosed in Rajavel, Han or Mitra, either taken individually or together assuming that someone would have been motivated to combine the teachings of these three patents, two in Class 257/442 and one in Class 420/523 for nanocrystals, to show that the specific quaternary compounds disclosed and Claimed by Applicants would overcome the problem of lattice matching to a tertiary mercury compound. Applicant's Invention as Claimed is drawn to a silicon based substrate and a specific epitaxially grown film e.g., $Cd_{1-z}Zn_zX_xX'_{1-x}$ as in Claim 1. It is not an issue of the overlapping of ranges as the Examiner indicated. It is a question of whether anyone would have been motivated to epitaxially grow an epitaxial film of the claimed quaternary compound or certain specific tertiary based compound such as CdS_xTe_{1-x} as Claimed in Claim 28, on a silicon based substrate in the first instance, when Rajavel itself teaches away the epitaxial growth/deposition of such compounds on an a silicon substrate due to tensile stress and the generation of dislocations in the detector structure which degrade performance, see Rajavel, Column 2, lines 3-16.

Since Applicant believes that Claims 1, 21 and 28 are Allowable, The Examiner's Rejection of Claim 4 based on a passivating layer, of Claim 6 for the use of silicon as a single crystal substrate, and to Claims 6-10, 15-18, 22, 26, 29 and 33 all of which Depend either directly or indirectly from either Claim 1 (Claims 4, 6-10, and 15-18) Claim 21 (Claims 22, and 26) or Claim 28 (as Amended in the Preliminary Amendment) (Claims 29 and 33). Likewise, Claims 11-12, 23, 24 and 30 also Depending directly or indirectly from Claim 1 (Claims 11-12), Claim 21 (Claims 23, 24) and Claim 28 (Claim 30) are also allowable whether or not a surface defect density would be is inherent in or unpatentable over the prior art by itself. Similarly, Claims 13-14, 19, 20, 24, 25, 31, 32 and Claims Depending from these Claims Depending from claim 1 (Claims 13-14 and 20), Claim 21 (Claims 24 and 25) or Claim 28 (Claims 31 and 32) are Allowable whether or not an overlayer would in and of itself be Patentable. Likewise, Claims 27 Depending from Claim 21 and Claim 34 Depending from Claim 28 are patentable if the base claim from which they Depend is Allowable.

Conclusion

Other than the issue of the confusion over whether Applicant's Application was Examined in view of the Preliminary Amendment Filed 27 May 2004 and the apparent separation of the Chen, *et al.* article also Filed by Applicant on 27 May 2004; Applicant believes that it has demonstrated that there would be no motivation on the part of a person of ordinary skill in the art to combine the references cited by the Examiner or to grow the Claimed quaternary or tertiary compounds Claimed by Applicant on a silicon based substrate due to well known problems in prior art methods of producing epitaxially grown compounds.

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Having Obviated each and every one of the Examiner's Rejections Applicant, Respectfully requests that the Examiner recognize the Amendments made by the Preliminary Amendment, enter Amendments made herein and grant Allowance of the Application.

The Examiner is invited to telephone the undersigned at the local telephone number given below if, after considering this Amendment, the Examiner is of the opinion that the Amendments made by Applicant in this Amendment or in the Preliminary Amendment have not resolved all outstanding issues in this case and brought the case into Condition for Allowance.

Respectfully submitted,

16 JANUARY 2007
DATE

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MBE growth of CdSeTe/Si composite substrate for long-wavelength IR HgCdTe applications

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Abstract

For the first time, the ternary alloy $CdSe_xTe_{1-x}(2\,1\,1)$ has been grown on $Si(2\,1\,1)$ substrates using molecular beam epitaxy. The growth of CdSeTe was facilitated using a compound CdTe effusion source and a Se effusion source. The alloy composition (x) of $CdSe_xTe_{1-x}$ ternary compound was controlled through the Se/CdTe flux ratio. Our results indicate that the quality of CdSeTe decreases as the alloy composition increases, which was possibly due to an alloy disordering effect. A similar trend was observed for the ternary alloy system CdZnTe. However, the alloy disordering effect in CdSeTe is less severe than that in CdZnTe. We have carried out the growth of CdSeTe on Si at different temperatures. Based on our results, we found that the rate of Se incorporation is higher than the rate of Te incorporation as growth temperature increases. As-grown CdSeTe with 4% Se, which is lattice matched to long-wavelength infrared HgCdTe material, exhibits excellent surface morphology, low surface defect density (less than $500\,cm^{-2}$) and low X-ray (full-width at half maximum) of 103 arcsec.

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PACS: 68.55.–a; 81.05.Dz; 81.15.Hi

Keywords: A3. Molecular beam epitaxy; B1. CdSeTe; B1. HgCdTe; B1. Si; B2. Long-wave infrared materials

1. Introduction

For over a decade, the HgCdTe research community has spent considerable effort to establish molecular beam epitaxial (MBE) growth of CdTe/Si composite substrates for HgCdTe material growth and infrared device applications [1–7]. As such, these research efforts have led to a relatively mature process for CdTe/Si. CdTe/Si substrates have been used to fabricate large-format short wavelength (SWIR) and medium wavelength (MWIR) HgCdTe infrared focal plane arrays [8,9]. However, even with the tremendous advancements made in CdTe/Si material quality over the years, exact lattice matching to HgCdTe is needed for long-wave (LWIR) material growth in order to reduce the dislocation density to a level suitable for LWIR device fabrication. This constraint is not as stringent for SWIR and MWIR material due to the inherently larger band gaps in those

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materials. To mitigate the lattice mismatch issue, initial effort was focused on incorporating 4.3% Zn into the CdTe/Si layer. However, we observed that CdZnTe/Si layers with lower defects and suitable crystal quality are difficult to achieve. Furthermore, it has been shown that the degradation of crystalline structure of $Cd_{1-y}Zn_yTe$ occurs for increasing Zn composition due to a miscibility gap [10]. In this work, we investigated an alternative material system, $CdSe_xTe_{1-x}/Si$, for lattice-matched composite substrate growth. A preliminary comparison between cation and anion mixing in CdTe based ternary compounds is made. In addition to its possible application for LWIR HgCdTe, II-VI compounds belonging to the cadmium chalcogenides family have the potential use for X-ray and gamma-ray detectors [11].

2. Experimental procedure

Growth of $CdSe_xTe_{1-x}$ on Si was conducted using a DCA MBE system equipped with a 3.25-in substrate heater. Three-inch Si(2 1 1) nominal wafers were used as substrates. All Si wafers were cleaned using the modified RCA process. This process leaves an approximate 12 Å uniform oxide layer on the Si surface, which must be thermally removed in the growth chamber. For these experiments, the samples were quickly heated to 1050°C to remove the oxide layer and then quickly cooled under an As_4 flux to 500°C. Finally, the sample was cooled to the nucleation temperature of 340°C without any flux. Note, that all temperatures stated are the reading of a thermocouple, which is located approximately 10 mm from the back of the substrate. Although the thermocouple does not measure the precise temperature of the sample surface, this configuration provides both excellent temperature control and run-to-run reproducibility.

After we removed the oxide layer and passivated the sample with As, a thick CdTe layer was grown using our standard process. This process starts with a seeding layer of thin ZnTe deposited at 340°C on Si substrate utilizing migration-enhanced epitaxy (MEE) [5] with elemental Zn and Te sources. After annealing the ZnTe layer at

490°C with Te flux for 20 min, a thick (~6 μm) CdTe layer was grown using a CdTe compound source. The growth rate of CdTe is approximately 0.75 μm h⁻¹. Periodically, during CdTe growth, the layer was briefly annealed to 530°C under a Te over pressure. This type of flash annealing was used to improve the CdTe layer quality. Finally $CdSe_xTe_{1-x}$ was grown on top of the CdTe layer using the CdTe compound source and an elemental Se source. For these experiments, no annealing sequences were utilized during CdSeTe growth. CdTe and CdSeTe growth temperatures were identical and were varied between 320°C and 440°C for this study.

3. Results and discussion

As-grown $CdSe_xTe_{1-x}$ layers were evaluated utilizing X-ray rocking curve measurements in order to gauge the overall crystalline quality. Additionally, we used X-ray diffraction to calculate the composition of the CdSeTe layer by determining the offset of the CdSeTe peak with respect to the position of the CdTe peak and assuming a linear relationship between alloy composition and $CdSe_xTe_{1-x}$ lattice constant. Such a linear relationship has been confirmed for $CdSe_xTe_{1-x}$ polycrystalline films deposited on glass using electron beam evaporation [12]. Based on these assumptions, we calculated that 4.0% Se incorporation is needed in CdTe to achieve lattice matching with LWIR $Hg_{0.78}Cd_{0.22}Te$.

To properly control the Se concentration, careful flux measurements of the Se source and the CdTe source were made prior to each MBE growth run using a retractable ion gauge placed in the sample growth position. We found that the Se concentration in CdSeTe follows quite linearly with the flux ratio of Se to CdTe, as is shown in Fig. 1. Although the goal was to grow $CdSe_{0.04}Te_{0.96}/Si$, a range of layer compositions was also grown in order to gauge material characteristics with respect to Se composition. In general, we observed the broadening of X-ray full-width at half-maximum (FWHM) of the CdSeTe layers from 70 to 230 arcsec as the Se concentration increases from 0% to 10%, respectively. In
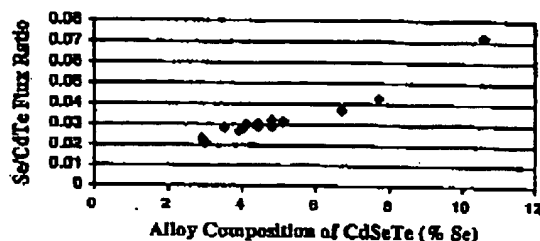
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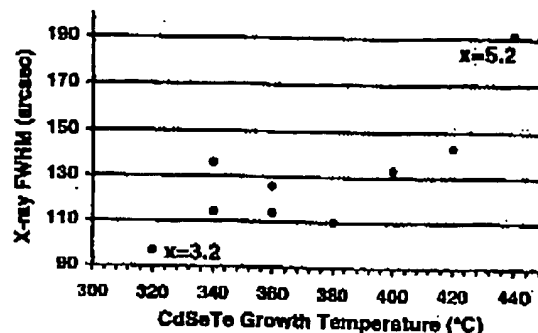Fig. 1. Se concentration in CdSeTe alloy as a function of Se/CdTe flux ratio.

Fig. 2. X-ray FWHMs of CdSeTe layers, with Se composition raging from 3.8% to 4.4% vs. CdSeTe growth temperature.

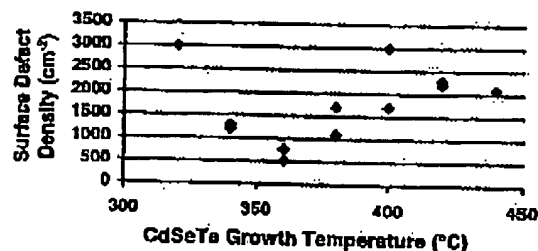Fig. 3. Surface defect density of as-grown CdSeTe/Si as a function of CdSeTe growth temperature.

our previous studies, we also observed broadening of X-ray FWHM of CdZnTe varies from 70 to 360 arcsec as the Zn concentration increases from 0% to 10% respectively. Broadening of X-ray FWHM in alloys such as CdZnTe and CdSeTe is usually related to the alloy disordering. From this measurement, it appears that the alloy disordering is much less severe in the CdSeTe alloy than in the CdZnTe alloy.

In order to study the Se incorporation in CdTe layers and to optimize the growth conditions for CdSeTe on Si, we investigated the growth of CdSeTe on CdTe/ZnTe/Si at different temperatures ranging from 320°C to 440°C. We evaluated the as-grown CdSeTe/CdTe/ZnTe/Si layers by X-ray diffraction and optical microscopy to determine the crystalline quality, alloy composition, surface morphology and surface defects. Fig. 2 shows the X-ray FWHMs of CdSeTe layers as a function of the CdSeTe growth temperatures, which exhibits a trend of slightly increasing X-ray FWHM as the growth temperature increases. Similar trends were also observed for surface defects and surface morphology as a function of CdSeTe growth temperature, as are shown in Figs. 3 and 4. The surface morphology of CdSeTe seems quite sensitive to the growth temperature, which becomes significantly rougher as the growth temperature increases. Our results indicate that the growth of good CdSeTe layers can be achieved in a growth window of 340-420°C, indicated by the thermocouple reading, which is larger than we expected. However, best CdSeTe layers were grown at the lower end of the growth window (340-380°C).

Additionally, we conducted a detailed study of Se incorporation in CdTe as a function of growth temperature. Since CdSeTe was grown using CdTe + Se fluxes, the growth occurs under (Se,Te)-rich conditions. During the growth, Se and Te are in competition for the same nucleation sites. If we assume that all the Cd atoms impinging on the substrate were incorporated, the maximum number of Se and Te atoms incorporated should be equal to the number of Cd atoms, which is proportional to the Cd flux. Since we are using a single CdTe cell to provide Cd and Te flux, we expect equal numbers of Cd and Te atoms due to the congruent evaporation of the II–VI compound. If we assume total incorporation of incoming Se atoms into the CdSeTe layer, the alloy composition of the ternary compound can be calculated as $x(\text{cal}) = \Phi_{Se}/(\Phi_{Se} + \Phi_{Te})_{incorporated}$. Since $(\Phi_{Se} + \Phi_{Te})_{incorporated} = \Phi_{Cd} = \Phi_{CdTe}/2$, therefore, $x(\text{cal}) = \Phi_{Se}/\Phi_{Cd} = 2\Phi_{Se}/\Phi_{CdTe}$, where Φ is the
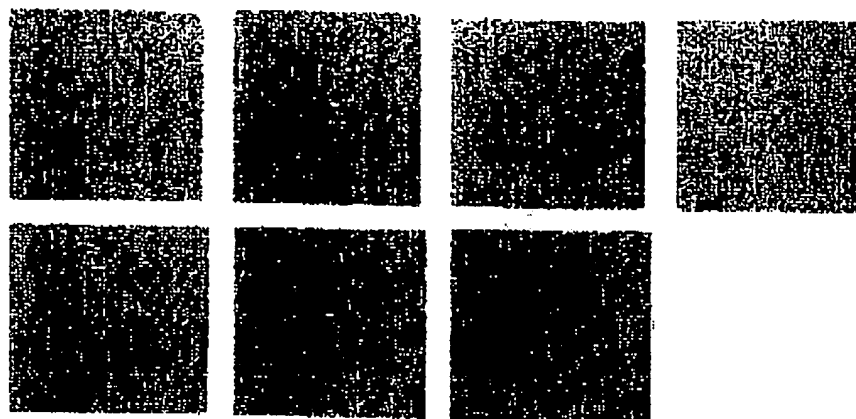
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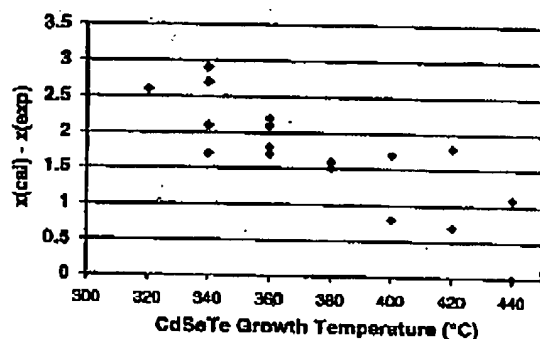Fig. 4. Surface morphologies of as-grown CdSeTe/Si layers grown at different temperatures.

Fig. 5. Difference between calculated and measured x values of CdSeTe alloy as a function of growth temperature.

material flux, measured by a nude ion gauge. We have measured the alloy compositions of many CdSeTe layers using X-ray diffraction and have found that the measured alloy composition is consistently smaller than the values derived from the Se/Te flux ratio calculation. Fig. 5 shows the difference in Se concentration between calculated and experimentally measured values (x(cal)–x(exp)) as a function of growth temperature. It is obvious that in the entire range of the growth window there exists a difference between calculated and measured values of the CdSeTe alloy. Additionally, this difference is always positive, which implies that not all Se atoms impinging on the CdSeTe

surface are incorporated as a result of competition between Te and Se atoms. However, the difference in the calculated and measured x value decreases as the growth temperature increases, which seems to suggest that the rate of selenium incorporation is relatively higher than the rate of tellurium incorporation as the growth temperature increases. An understanding of this effect can be obtained if we consider that the formation of the CdSeTe epilayer is occurring through various rate competitions between the binary compounds CdSe and CdTe. Since the bond length of CdSe is shorter than that of CdTe, it is expected that binding energy of CdSe is greater than the binding energy of CdTe. Additionally, the heats of formation and atomization for CdSe are 32.5 and $57 \, kcal^{-1} g \, atom^{-1}$, and the heats of formation and atomization for CdTe are 23.8 and $48 \, kcal^{-1} g \, atom^{-1}$, respectively [13]. Based on these data, the CdSe binary system should be more stable at higher temperatures than the CdTe binary system, and thus it can be understood why the incorporation of selenium increases with the growth temperature. A similar trend has been observed by Turco-Sandroff and his co-workers in the case of MBE growth of ZnSeTe [14]. They also found that the difference between calculated and measured x values of ZnSeTe alloys was almost eliminated when ZnSeTe was grown under Zn-rich condition. It is certainly interesting to study
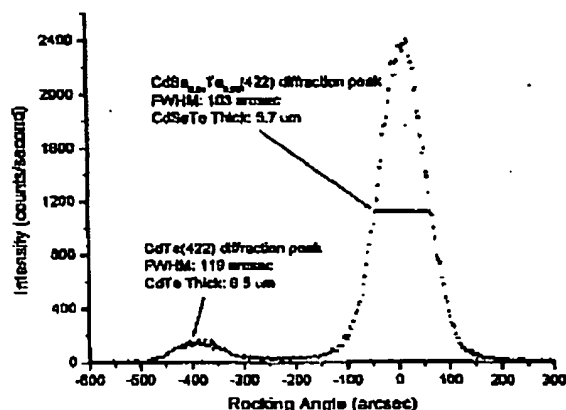
Fig. 6. X-ray rocking curve of a CdSeTe(211)/CdTe/ZnTe/Si wafer with 4% Se concentration.

the growth of CdSeTe under Cd-rich conditions and the growth of CdSe as a function of growth temperature. The results of such study will be published later.

We have observed that the X-ray FWHM will generally increase as the *x* value of CdSeTe alloy increases. Fortunately, only 4% of Se is needed in CdSeTe composite substrate to lattice match with LWIR-HgCdTe. The as-grown CdSeTe with 4% Se exhibits excellent surface morphology and high crystalline quality. Fig. 6 records an X-ray rocking curve of a 3-in $CdSe_{0.04}Te_{0.96}$/Si layer. The FWHM of a 5.8-μm $CdSe_{0.04}Te_{0.96}$ layer is 103 arcsec. To our knowledge, this is the lowest value that has ever been reported for Si-based composite substrate lattice matched to LWIR HgCdTe.

4. Conclusions

We have reported for the first time the successful MBE growth of CdSeTe on Si lattice matched to LWIR HgCdTe. CdSeTe with 4% Se incorporated exhibits excellent surface morphology, low surface

defect density and an X-ray FWHM of 103 arcsec. The growth of CdSeTe was achieved using a CdTe compound source and an elemental Se source. Alloy composition can be controlled by the Se/CdTe flux ratio and the rate of Se incorporation is determined to be higher than the rate of Te incorporation as the growth temperature increases.

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